



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,203	07/03/2003	Gurtej S. Sandhu	303.931US2	4599
21186	7590	07/20/2010	EXAMINER	
SCHWEGMAN, LUNDBERG & WOESSNER, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			MALDONADO, JULIO J	
			ART UNIT	PAPER NUMBER
			2823	
			NOTIFICATION DATE	DELIVERY MODE
			07/20/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@slwip.com
request@slwip.com

Office Action Summary	Application No.	Applicant(s)	
	10/613,203	SANDHU ET AL.	
	Examiner	Art Unit	
	JULIO J. MALDONADO	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 16 June 2010.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-9, 11-13, 52, 53 and 62-70 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-9, 11-13, 52, 53 and 62-70 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

1. The cancellation of claim 10, 14-51 and 54-61 as set forth in the reply filed on 06/16/2010 is acknowledged.
2. Claims 1-9, 11-13, 52, 53 and 62-70 are pending in the application.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/16/2010 has been entered.

Claim Objections

4. Claim 8 is objected to because of the following informalities: In claim 8, line 11, where the applicants recite, "the support surface...into the recess...", change --a support surface...into a recess--. Appropriate correction is required.
5. Claim 11 is objected to because of the following informalities: claim 11 depends from cancelled claim 10. Appropriate correction is required.
6. In reply filed on 02/17/2010, claim 11 depends on claim 10, which depends on independent claim 8. For purposes of this office action, claim 11 is read as depending on claim 8.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al. (U.S. 5,489,548, hereinafter Nishioka) in view of Fazan et al. (U.S. 5,392,189, hereinafter Fazan).

In reference to claim 1, Nishioka (See Fig.12-14, for example) discloses a substrate assembly comprising a support surface (42) having a uniform composition and extending into a recess formed in a substrate (30, 32); a conductive layer (46) spaced apart from the support surface (42); and a plurality of high-k dielectric layers (44) positioned between the support surface (42) and the conductive layer (46), including a first high-k dielectric layer, and a second high-k dielectric layer including deposited components different from those in the first high-k dielectric layer (Nishioka, column 9, lines 23 – 36) and wherein the support surface (42) remains substantially free of an oxide present in the plurality of high-k dielectric layers (44) (Nishioka, column 4, lines 8 – 14 and column 5, line 32 – column 9, line 55).

Still, Nishioka fails to disclose a support surface and the conductive layer extending into a recess formed in the substrate assembly.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the

support surface (85) extend into a recess formed in a substrate assembly, and wherein in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer (89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nishioka and Fazan to enable substituting the support substrate of Nishioka with an equivalent support substrate as disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

In reference to claim 2, the combination of Nishioka and Fazan discloses wherein said plurality of high-k dielectric layers comprises a first high-k dielectric layer contacting said support surface (Nishioka, see Figs.12-14).

In reference to claim 3, the combination of Nishioka and Fazan discloses a barrier layer (52) between said support surface and said plurality of high-k dielectric layers (Nishioka, column 7, lines 30 – 40).

In reference to claim 4, the combination of Nishioka and Fazan discloses wherein said support surface is a capacitor electrode (Nishioka, column 4, lines 8 – 14 and column 5, line 32 – column 9, line 55).

In reference to claim 12, Nishioka (See Fig.12-14, for example) discloses a substrate assembly comprising a first high-K capacitor dielectric comprising tantalum pentoxide; a second high-K capacitor dielectric comprising a high-K dielectric having at least one different component than the first high-K capacitor dielectric and contacting said first high-K capacitor dielectric, wherein said first high-K capacitor dielectric and said second high-K capacitor dielectric are oxides, a support surface (42) having a uniform composition and that remains substantially free of the oxides; and a conductive layer (46) spaced apart from the support surface (42), wherein the first high-K capacitor dielectric and the second high-K capacitor dielectric abut the support surface (42) and the conductive layer (46) (Nishioka, column 4, lines 8 – 14 and column 5, line 32 – column 9, line 55).

Still, Nishioka fails to disclose a support surface and the conductive layer extending into a recess formed in the substrate assembly.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the support surface (85) extend into a recess formed in a substrate assembly, and wherein

in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer (89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nishioka and Fazan to enable substituting the support substrate of Nishioka with an equivalent support substrate as disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

9. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka ('548) in view of Fazan ('189) as applied to claims 1-4 and 12 above, and further in view of Park et al. (U.S. 5,837,593, hereinafter Park).

The combination of Nishioka and Fazan substantially discloses all aspects of the claimed invention, but fails to expressly disclose wherein said plurality of high-k dielectric layers defines a thickness of at most 200 angstroms; wherein said plurality of high-k dielectric layers comprises a first high-k dielectric defining a thickness of at least a monolayer; and wherein said first high-k dielectric layer defines a thickness of at least 10 angstroms.

However, Park (Fig.2E) discloses a related semiconductor device including a support surface (40); a conductive layer (46) spaced apart from the support surface (40); and a plurality of high-k dielectric layers (42, 44) positioned between the support surface and the conductive layer (46), wherein the plurality of high-k dielectric layers (42, 44) includes a first high-k dielectric layer (44) defining a thickness of 45 angstroms, and wherein the plurality of high-k dielectric layers defines a thickness about 85 angstroms (Park, column 5, lines 21 - 61).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nishioka and Fazan with Park to enable the plurality of high-k dielectric layers of Nishioka and Fazan to have the thicknesses defined in Park because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful dielectric layers with a desired thickness in Nishioka and Fazan and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07), and furthermore, because the fact that the claimed combination of elements was “obvious to try” might show that such combination was obvious under 35 U.S.C. §103, since, if there is design need or market pressure to

solve problem, and there are finite number of identified, predictable solutions, person of ordinary skill in art has good reason to pursue known options within his or her technical grasp, and if this leads to anticipated success, it is likely product of ordinary skill and common sense, not innovation (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

10. Claims 8, 9, 11, 52, 53 and 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (U.S. 5,837,593, hereinafter Park) in view of Fazan et al. (U.S. 5,392,189, hereinafter Fazan).

In reference to claim 8, Park (Fig.2E) discloses a capacitor dielectric including a first high-k capacitor dielectric (42) comprising tantalum pentoxide; a second high-k capacitor dielectric (44) contacting said first high-k capacitor dielectric (42) and comprising tantalum pentoxide; and a conductive layer (46) spaced apart from the support surface (40), wherein the first high-k capacitor dielectric (42) and the second high-k capacitor dielectric (44) abut the support surface (40) and the conductive layer (46) (Park, column 4, line 40 – column 6, line 5).

Park fails to disclose wherein the conductive layer extends into a recess.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the support surface (85) extend into a recess formed in a substrate assembly, and wherein in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced

apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer (89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nishioka and Fazan to enable substituting the support substrate of Nishioka with an equivalent support substrate as disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

In reference to claim 9, the combination of Park and Fazan discloses wherein said first high-k capacitor dielectric defines a first thickness, and wherein said second high-k capacitor dielectric defines a second thickness that is different from said first thickness (Park, column 5, lines 21 - 50).

In reference to claim 11, the combination of Park and Fazan discloses wherein said first high-k dielectric oxide is a first oxide, and wherein said second high-k capacitor dielectric is a second oxide different in thickness form said first oxide (Park, column 5,

lines 21 - 60). Therefore, the combination of Park and Fazan encompasses the recited limitation.

In reference to claims 52 and 53, Park (Fig.2E) discloses a capacitor dielectric (42, 44), comprising a plurality of capacitor dielectric layers (42, 44) defining a total thickness ranging from 50 to 1000 angstroms, wherein each layer of said plurality is a tantalum pentoxide high-K dielectric defining an individual thickness, further wherein a supporting surface (40) abuts the plurality of capacitor dielectric layers (42, 44) remains substantially free of the metal oxide (Park, column 2, lines 46 – 55), and an electrode layer (46) is disposed over the plurality of dielectric layers (42, 44) (Park column 3, lines 24 – 45 and column 4, line 50 – column 6, line 5).

Park fails to expressly disclose wherein the plurality of capacitor dielectric layers defines a thickness from 50 to 70 angstroms. However, in the case where the claimed ranges “overlap or lie inside ranges disclosed by the prior art” a *prima facie* case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the thickness disclosed in Park to arrive at the recited limitation.

Park fails to expressly disclose wherein the plurality of dielectric layers defines an individual thickness ranging from 10 to 40 angstroms, and wherein at least a lowest layer of said plurality defines an individual thickness of about 20 angstroms.

One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to obtain a desired plurality of dielectric layers with a desired level of leakage reduction. Applicant has not disclosed

that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears *prima facie* that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Park fails to disclose wherein the support surface and the conductive layer extend into a recess.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the support surface (85) extend into a recess formed in a substrate assembly, and wherein in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer

(89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nishioka and Fazan to enable substituting the support substrate of Nishioka with an equivalent support substrate as disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

In reference to claim 67 Park (Fig.2E) discloses a capacitor dielectric (42, 44), comprising a plurality of capacitor dielectric layers (42, 44) abutting a supporting surface (40) having a uniform composition and an electrode layer (46), wherein each layer of the plurality (42, 44) is a high-k dielectric, wherein each layer of the plurality is a tantalum pentoxide layer, wherein a first tantalum pentoxide layer (42) is formed using one oxidation step, and a second tantalum pentoxide (44) layer is formed using two oxidation steps, wherein an underlying layer includes a means to minimize oxidation beyond the plurality of capacitor dielectric layers, further wherein the tantalum pentoxide is not diffused from the plurality of the high-k dielectric layer into the supporting surface extending into the recess and adjacent the plurality of layers (Park, column 2, line 46 – column 6, line 5).

Park fails to expressly disclose wherein at least one layer of the plurality manifests a greater oxidation than would an equal thickness of an underlying layer of the plurality.

However, Park discloses wherein a first tantalum pentoxide layer is formed using one oxidation step, and a second tantalum pentoxide layer is formed using two oxidation steps (Park, column 5, lines 21 – 60). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the second tantalum pentoxide layer manifest greater oxidation than the first tantalum pentoxide layer because it is exposed to two oxidation steps. Therefore, the recitation is obvious over Park.

Park fails to disclose wherein the support surface and the conductive layer extend into a recess.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the support surface (85) extend into a recess formed in a substrate assembly, and wherein in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer

(89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nishioka and Fazan to enable substituting the support substrate of Nishioka with an equivalent support substrate as disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

In reference to claim 68, the combination of Park and Fazan discloses wherein the plurality of capacitor dielectric layers defines a total thickness that ranges between approximately 50 to 1000 angstroms.

The combination of Park and Fazan fails to expressly disclose wherein the plurality of capacitor dielectric layers defines a thickness from 50 to 70 angstroms.

However, in the case where the claimed ranges “overlap or lie inside ranges disclosed by the prior art” a *prima facie* case of obviousness exists. MPEP 2144.05.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the thickness disclosed in Park to arrive at the recited limitation.

In reference to claims 69 and 70, the combination of Park and Fazan substantially discloses all aspects of the invention but fails to expressly disclose wherein the plurality of dielectric layers defines an individual thickness ranging from 10 to 40 angstroms, and wherein at least a lowest layer of said plurality defines an individual thickness of about 20 angstroms.

One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to obtain a desired plurality of dielectric layers with a desired level of leakage reduction. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

11. Claims 13 and 62-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takehiro et al. (U.S. 6,403,441 B1, hereinafter Takehiro) in view of Fazan et al. (U.S. 5,392,189, hereinafter Fazan).

In reference to claim 13, Takehiro (Figs.2d, 4a and 4b) discloses a capacitor structure, comprising a first electrode layer (6) having a uniform composition; a dielectric layer (9, 10, 11) disposed over said first electrode layer (6), wherein said dielectric layer (9, 10, 11) comprises a plurality of consecutively-positioned sub-layers, wherein each of said sub-layers comprises a high-dielectric-constant material, wherein said dielectric layer comprises an element common to all sub-layers of said plurality, wherein the dielectric layer (9, 10, 11) further includes a oxygen diffusion barrier layer (10) that prevents oxides to be formed in said first electrode layer (6) wherein one of said sub-layers has more oxygen, defined by point A (Takehiro, Fig.4b) than another of said sublayers defined by point B (Takehiro, Fig.4b); and a second electrode layer (8) disposed over said dielectric layer (9, 10, 11), wherein the invention may be carried out in any semiconductor device as long as it has a capacitor structure that employs a highly dielectric film as an insulating film and wherein at least one of the sub-layers includes a deposited component (see Fig.4(b)), labeled dielectric component, different from one or more of the other sub-layers (Takehiro, column 4, lines 46 – 54, column 6, line 16 – column 8, line 27 and column 16, lines 29 – 35).

Takehiro fails to expressly disclose wherein one of the sub-layers of the dielectric layer manifests greater oxidation than would an equivalent thickness of an underlying sub-layer of the dielectric layer further

However, the recitation of “greater oxidation” is seen to be a recitation of a dielectric layer of said plurality of layers having a higher concentration of oxygen with respect to another layer of said plurality. Therefore, Takehiro teaches the claimed limitation because Takehiro discloses an overlying dielectric layer having a lower concentration.

Still, Takehiro fails to disclose, wherein the first electrode having said uniform composition and the second electrode extend into a recesses formed in the substrate assembly.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the support surface (85) extend into a recess formed in a substrate assembly, and wherein in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer (89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Takehiro and Fazan to enable substituting the support substrate of Takehiro with an equivalent support substrate as

disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

In reference to claim 62, Takehiro (Figs.2d, 4a and 4b) discloses a capacitor structure, including a first electrode (6) having a uniform composition, a capacitor dielectric and a second electrode (8), wherein said second electrode (8) is spaced apart from the first electrode and said capacitor dielectric abuts said first (6) and second (8) electrode, wherein said capacitor dielectric comprises a plurality of capacitor dielectric layers (9, 10, 11), wherein each layer of said plurality is a high-K dielectric defining an individual thickness, wherein at least one layer of the plurality has a greater concentration of oxygen (Fig.4b, Point A) than an underlying layer (Figs.4b, Point B), and wherein said capacitor dielectric (9, 10, 11) further includes an oxygen barrier layer (10) that prevents oxides from forming in a support surface (6) (Takehiro, column 4, lines 46 – 54 and column 6, line 16 – column 8, line 27). Furthermore, Takehiro discloses wherein the one of the dielectric layers (9) defines a thickness of, for example, 10 nm and another of the dielectric layers (11) defines a thickness of, for example, 40 nm, and wherein the invention is not restricted to these examples (Takehiro, column 16, lines 17 – 35), wherein the invention may be carried out in any semiconductor device as long as it has a capacitor structure that employs a highly dielectric film as an insulating

film (Takehiro, column 16, lines 29 – 35) and wherein at least one of the sub-layers includes a deposited component (see Fig.4(b)), labeled dielectric component, different from one or more of the other sub-layers.

Takehiro fails to expressly disclose wherein at least one layer of the plurality manifests a greater oxidation than would an equal thickness of an underlying layer of the plurality.

However, the recitation of “greater oxidation” is seen to be a recitation of a dielectric layer of said plurality of layers having a higher concentration of oxygen with respect to another layer of said plurality. Therefore, Takehiro teaches the claimed limitation because Takehiro discloses an overlying dielectric layer having a lower concentration.

Still, Takehiro fails to disclose, wherein the first and second electrodes extend into a recesses formed in the substrate assembly.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the support surface (85) extend into a recess formed in a substrate assembly, and wherein in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer

(89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Takehiro and Fazan to enable substituting the support substrate of Takehiro with an equivalent support substrate as disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

Still, the combination of Takehiro and Fazan fails to expressly disclose wherein said plurality of capacitor dielectric layers defines a total thickness ranging from 50 to 70 angstroms, wherein each layer of said plurality defines an individual thickness ranging from 10 to 40 angstroms in thickness, and wherein at least a lowest layer of said plurality defines an individual thickness of about 20 angstroms.

One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to obtain a desired plurality of dielectric layers. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears *prima facie* that the process would possess utility using another dimension (Instant specification, page 10, line 13 – page 11, line 4). Indeed, it has been held that

mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the combination of Takehiro and Fazan to arrive at the claimed invention through routine optimization.

In reference to claim 63, Takehiro (Figs.2d, 4a and 4b) discloses a capacitor structure, including a first electrode (6) having a uniform composition, a capacitor dielectric and a second electrode (8), wherein said second electrode (8) is spaced apart from the first electrode and said capacitor dielectric abuts said first (6) and second (8) electrode, wherein said capacitor structure comprises a plurality of capacitor dielectric layers (9, 10, 11), wherein each layer of the plurality is a high-K dielectric, wherein at least one layer of the plurality has a greater concentration of oxygen (Fig.4b, Point A) than an underlying layer (Figs.4b, Point B), wherein said capacitor dielectric (9, 10, 11) further includes an oxygen barrier layer (10) that prevents oxides from forming in a support surface (6), wherein the invention may be carried out in any semiconductor device as long as it has a capacitor structure that employs a highly dielectric film as an insulating film (Takehiro, column 4, lines 46 – 54, column 6, line 16 – column 8, line 27

and column 16, lines 29 – 35) and wherein at least one of the sub-layers includes a component (see Fig.4(b)), labeled dielectric component, different from one or more of the other sub-layers.

Takehiro fails to expressly disclose wherein one of the sub-layers of the dielectric layer manifests greater oxidation than would an equivalent thickness of an underlying sub-layer of the dielectric layer.

However, the recitation of “greater oxidation” is seen to be a recitation of a dielectric layer of said plurality of layers having a higher concentration of oxygen with respect to another layer of said plurality. Therefore, Takehiro teaches the claimed limitation because Takehiro discloses an overlying dielectric layer having a lower oxygen concentration.

Still, Takehiro fails to disclose, wherein the first electrode and the second electrode extend into a recesses formed in the substrate assembly.

However, Fazan (Figs.14A-15B) discloses a substrate assembly including a support surface (85) having a uniform composition and wherein in one embodiment, the support surface (85) extend into a recess formed in a substrate assembly, and wherein in another embodiment, the support surface (85) does not extend into a recess; a high-k dielectric layer (87) over said support surface (85); and a conductive layer (89) spaced apart from the support surface (85) and abutting said high-k dielectric layer (87) and said support surface (89), wherein in one embodiment said support surface (85) and said conductive layer (89) do not extend into a recess formed in a substrate, and wherein in a second embodiment said support surface (85) and said conductive layer

(89) extend into a recess formed in the substrate assembly (Fazan, column 7, line 7 – column 8, line 64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Takehiro and Fazan to enable substituting the support substrate of Takehiro with an equivalent support substrate as disclosed in Fazan, because is *prima facie* obvious to combine equivalents known for the same purpose (see MPEP 2144.06, I and II), and furthermore, because variations of particular work available in one field of endeavor may be prompted by design incentives and other market forces, either in same field or different one, and if person of ordinary skill in art can implement predictable variation, 35 U.S.C. §103 likely bars its patentability (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)).

In reference to claims 64-66, the combination of Takehiro and Fazan discloses wherein the one of the dielectric layers defines a thickness of, for example, 10 nm and another of the dielectric layers defines a thickness of, for example, 40 nm, and wherein the invention is not restricted to these examples (Takehiro, column 16, lines 17 – 35).

The combination of Takehiro and Fazan fails to expressly disclose wherein said plurality of high-k dielectric layers defines a thickness of at most 200 angstroms; wherein said plurality of high-k dielectric layers comprises a first high-k dielectric layer contacting said support surface and defining a thickness of at least a monolayer; wherein said first high-k dielectric layer defines a thickness of at least 10 angstroms; wherein the plurality of capacitor dielectric layers defines a total thickness that ranges between approximately 50 angstroms and approximately 70 angstroms; wherein each

layer of the plurality defines an individual layer thickness that ranges between approximately 10 angstroms and approximately 40 angstroms; and wherein at least a lowest layer of the plurality defines an individual thickness of approximately 20 angstroms.

One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to obtain a desired plurality of dielectric layers. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears *prima facie* that the process would possess utility using another dimension (Instant specification, page 10, line 13 – page 11, line 4). Indeed, it has been held that mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the combination of Takehiro and Fazan to arrive at the claimed invention through routine optimization.

Response to Arguments

12. Applicant's arguments filed 06/16/2010 have been fully considered but they are not persuasive.

The applicants argue, "...Applicants is unable to find in Takehiro a first high K dielectric layer, and a second high K dielectric layer including deposited components different from those in the first high K dielectric layer...".

In response to this argument, Takehiro, in Fig. 4(b) discloses wherein one of the layers, represented by point D includes ruthenium added by a previous deposition process. Therefore, Takehiro discloses a second high K dielectric layer including at least one deposited component different from those in the first high K dielectric layer, as disclosed in claims 12, 13, 62 and 63.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIO J. MALDONADO whose telephone number is (571)272-1864. The examiner can normally be reached on Mon-Fri, 8:00 A.M.-4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Julio J. Maldonado
Primary Examiner
Art Unit 2823

/Julio J. Maldonado/
Primary Examiner, Art Unit 2823